

Michael Joyner

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SUMMARY

Senior IC/PCB Layout Engineer with 45 years of industry experience, specializing in infrared ROIC's, CMOS image sensor design, and full chip integration w/ Tanner EDA tools and Calibre DRC/LVS back-end verification. IPC Certified Expert in PCB design and layout w/ Mentor PADS, Orcad, Altium Designer, and a robust patent portfolio from extensive work in video, consumer, medical, and military applications. Design Bureau Principal, Program and Product Manager, and CAE/CAD department manager. Introduced and developed new product concepts. Developed and administered documentation & process systems. Manage workgroups. Calibration, test & debug designs, optical bench & electronic engineering lab skills. Seeking to leverage deep technical and product expertise and innovative problem-solving skills in a Senior IC/PCB Layout Engineer or Product Development role.

- PCB work includes 2 layers to complex/constrained 24 layers, 0.05mm/0.075mm feature/space, high-speed, RF, matched differential busses, BGA's 1.00mm- 0.25mm, flex, and rigid-flex. Library/Librarian creation and editing.
- IC layout work includes mixed signal, low noise, and high-speed layout. 1.5um- 90nm nodes, power distribution mitigation, schematic entry, and full verification.
- Guest Lecturer @ Cornell University, fall semester PCB design series.
- Subject Matter Expert @Triple Crown Consulting, Austin, Texas.
- Space flight, radar, and communications RF PCB design. Altium toolsets

WORK EXPERIENCE

Town Line Technologies, LLC.

Cortland NY

President, Senior Principal & Layout Engineer

Jan 2013 - Present

- Leveraging 45 years of experience, managing and designing a diverse portfolio of IC and PCB layouts, testing, and consulting services across video, consumer, medical, military, and professional music industries.
- 26 years designing advanced CMOS image sensors, securing 81+ US and international patents in the field.
- Servicing 10-24 yr rigid flex HD camera projects, large Xilinx / Altera BGA's. 3g-10g interfaces. Mentor Pads VX Suite, Orcad Suite, Altium Designer -PCB design, Tanner EDA suite, Mentor Calibre for IC design.
- Military Contracts, projects including rigid flex HD camera/sensor systems. high-speed data interfaces, and fire control systems. S-Band, X-Band, K/Ka-Band RF. Medical devices include Electron Microscope imaging, High Speed Tomography, and Sensory Diagnostic instruments.
- High-Speed backplanes with peripheral monitoring >42GHz, high density assemblies.
- Aerospace systems, vision/imaging sensing w/downstream data management/processing, high density assemblies.

Senseseeker Engineering, INC.

Santa Barbara

Senior IC Layout Engineer

Nov 2022 - Mar 2024

- With Team multiuser environment, designed infrared ROIC's, CMOS image sensor layouts and schematic entry, ensured detailed specifications were met, utilizing Tanner EDA tools and Calibre DRC/LVS for verification.
- PCB design and layout in Altium Designer. Creation of mechanical drawings and supporting documents.

Panavision Imaging, LLC.

Homer NY

Co-Founder, Imager Design & Layout Engineer, Program Manager

Sep 1998 - Dec 2012

- Designed CMOS image/camera products adhering to diverse application requirements, including consumer electronics, professional cinema, and specialized military and industrial uses.
- Produced physical layouts of all company sensor products with "first silicon" working die Contributed to the development of innovative sensors, including a 60fps 8mp analog sensor and a high-speed >120fps 37mp sensor.
- Originated the concept, product requirements, and participated in the design of the industry's first programmable, reconfigurable wide linear image sensor, leading to volume production and commercial success.
- Resolved packaging issues with international vendors, significantly improving product yield from 68% to over 88%.
- Facilitated implementation and adoption of ISO9001 policies achieving certification.

Philips Broadband Networks

Manlius, NY

Senior Printed Circuit Board Designer

- Designed multi-layer, double-sided printed circuit boards optimized for through-hole and surface-mount technologies, adhering to high-volume design for manufacturability, DFM, and DFT standards.
- Contributed to the design of circuitry for cable TV and internet delivery products transitioning from 850 MHz to 1 GHz frequency range, including schematic entry, assembly drawings, and documentation creation.

CID Technologies

Liverpool, NY

Engineering Specialist

- Developed CAE/CAD designs for imager-based video cameras, for diverse military and aerospace applications.
- Designed embedded FPGA/PGA/PAL products, schematic entry simulation, and PCB layouts.
- Created prototypes, provided engineering support w/ testing, calibration, and comprehensive documentation.

Syracuse Scientific

Clay, NY

Engineering Technician

- Design electronic assemblies/test fixtures for vidicon based video cameras used in medical x-ray systems.
- Prepared and submitted comprehensive documentation for Underwriters Laboratories (UL) approval processes.
- Conducted testing and developed prototypes to a high standard, Testing and prototyping to presentation level

PATENTS

"A Video Bus For High Speed Multi-Resolution Imagers " 2003 Patent: US 6,590,198

"A Video Bus For High Speed Multi-Resolution Imagers And Method Thereof" 2003 Patents: (US) 6,633,029 (China) PCT/US01/02309 (European) PCT/US02/01864, PCT/US01/02309 (Japan) 2001-553588 (Taiwan) 90101651

"Scanning Image Employing Multiple Chips With Staggered Pixels" 2006 Patent: US 7,045,758

"Solid State Imager With Reduced Number Of Transistors Per Pixel" 2006 Patent: US 7,057,150

"Scanning imager employing multiple chips with staggered pixels" 2006 Patent: US 7,122,778 Oct-31-2006 Patent: 7,129,461 June-30-2009 Patent: 7,554,067, EP1878215 B1

"Image Sensor ADC and CDS per Column" 2011 Patent: US 7,903,159, CA2758275A1, CN102461158A, EP2417763A1

"Sub-Pixel Array Optical Sensor" Oct-11-2011 Patent: US 8,035,711

"Image sensor ADC and CDS per Column with Oversampling" 2012 Patent: US 8,169,517, CA2758275A1, CN102461158A, WO2010117462A1

"Color Pixel Pattern Scheme for High Dynamic Range Optical Sensor" -2009 Patent App: US 2009/0290052 A1

"Increasing The Resolution Of Color Sub-Pixel Arrays" 2010 Patent App: US 2007/0149393 A1, EP2540077A1, WO2011106461A1

"Variable Active Image Area Array Sensor" 2011 Patent App: WO 2011106461 A1, US 2011/0205384 A, CA2790853 A1, EP2539854A1

"Image sensor adaptive column readout structure" 2011 Patent Application: PCT/US2012/055575, WO2013040458 A1

PUBLICATIONS- TECHNICAL

"A CMOS video sensor for High Dynamic Range (HDR) imaging," 2008 42nd IEEE Asilomar Conference on Signals, Systems and Computers' Publication Date: 26-29 Oct.

"Broadcast quality 3840x2160 color imager operating at 30 fps," Proc. SPIE Vol. 5017-01. Jan 2003 Santa Clara, CA.

"Ultrahigh-speed CMOS scanning linear imager family," Proc. SPIE Vol. 4306 Jan 2001, San Jose, CA.

"CMOS sensors overcome bad image and early hype", Laser Focus World, July 1999, Penwell.

"1.5 FET per Pixel Standard CMOS Active Column Sensor", SPIE Vol. 3649-27, Jan 1999.

"Selectable One to Four Port Very, High speed 512 X 512 CID", SPIE, CCD and Solid State Optical Sensors Vol. 1447-18, February 1991, San Jose, CA.

PUBLICATIONS- BOOKS

J Ranch Wild Turkey Cuisine
Tales from the Roost
Reapercide: Fatalism Defined
A Walk In The Turkey Woods
One Percent 365

Random³ Musings: A Left
Hemisphere Reveal
Random² Musings: A Left
Hemisphere Continuum
Random Musings of the Left
Hemisphere

Ten To Life. Delirium Tales of a
Covid-19 Survivor
Grand Days in the Turkey Woods
Tales from the Turkey Woods
Hills of Truxton

Book details see: www.joyneroutdormedia.com

EDUCATION / TRAINING

- Coursiv Mastery AI Program
- Calibre, IC Layout Rule Writing - Mentor Graphics
- Virtuoso XL Layout - Cadence
- Tanner EDA Tools 2000 - Tanner Corp
- Practical Integrated Circuit Fabrication - Integrated Circuit Engineering (I.C.E)
- IPC Certified Interconnect Designer - C.I.D.,
Certified C.I.D.+ Adv. Certification
- PADS Layout & Logic Schematic - Pads Corp.
- PWB Design - IPC Designers Council
- AutoCad R13 - MicroCAD Managers
- TQM ISO9000 - RIT
- Microsoft Excel, Word, Frontpage – Phillips BB
- Workview+ - ViewLogic Systems
- Xact DM - Xilinx Corp.
- Maxplus, PGA Design - Altera Corp.
- Design Techniques for Controlling Radiated Emissions
- University of Wisconsin-Milwaukee
- EMI Compatibility Design Practices, System EMC -
University of Wisconsin-Milwaukee
- Grounding/Shielding for Electronic Instrumentation -
Missouri Rolla College
- Geometric Dimensioning Tolerancing - Shepherd Ind.
- Undergraduate Study - Onondaga Community College
- Math/Industrial Arts Major, North Syracuse HS

CERTIFICATIONS / PROFESSIONAL MEMBERSHIPS

- IPC Designers Council, #1021032
- IEEE Senior Member, #92567483
- SPIE Member, #350208
- New York State Outdoor Writers Association (NYSOWA), Past President, Active Member
- Association of Great Lakes Outdoor Writers (AGLOW) Active Member

VOLUNTEER EXPERIENCE

Board of Directors:

- IEEE Ithaca Section (2015-present), Past Section Chairman (2023-2025)
- New York Outdoor Writers Assoc. (NYSOWA) (2014-current) President (2016-2018)
- Cortland Main Street Music Series, Treasurer
- NY State Chapter National Wild Turkey Federation President
- CNY Chapter, Ruffed Grouse Society Vice President

Race Course & Technical Director:

- Willow Bay Women's Distance Festival (1994-present), supervise 20+ volunteers.
- Race for the Cure @ Syracuse supervised 120+ volunteers.
- Chemical Bank Challenge @ Syracuse supervised 80+ volunteers
- Syracuse Festival of Races, supervised 20+ volunteers.